NASA-DoD LEAD-FREE ELECTRONICS PROJECT: OVERVIEW

Kurt Kessel
ITB, Inc.
NASA Technology Evaluation for Environmental Risk Mitigation (TEERM) Principal Center
Kennedy Space Center, FL, USA
kurt.r.kessel@nasa.gov
{On behalf of the NASA-DoD Lead-Free Electronics Project Consortium}

ABSTRACT
Original Equipment Manufacturers (OEMs), depots, and support contractors have to be prepared to deal with an electronics supply chain that increasingly provides parts with lead-free finishes, some labeled no differently and intermingled with their SnPb counterparts. Allowance of lead-free components presents one of the greatest risks to the reliability of military and aerospace electronics. The introduction of components with lead-free terminations, termination finishes, or circuit boards presents a host of concerns to customers, suppliers, and maintainers of aerospace and military electronic systems such as:

1. Electrical shorting due to tin whiskers
2. Incompatibility of lead-free processes and parameters (including higher melting points of lead-free alloys) with other materials in the system
3. Unknown material properties and incompatibilities that could reduce solder joint reliability

As the transition to lead-free becomes a certain reality for military and aerospace applications, it will be critical to fully understand the implications of reworking lead-free assemblies.

Key words: lead-free, reliability, harsh environments testing, aerospace

BACKGROUND
The NASA-DoD Lead-Free Electronics Project builds on the results from the Joint Council on Aging Aircraft/Joint Group on Pollution Prevention (JCAA/JG-PP) Lead-Free Solder Project, the first group to test the reliability of lead-free solder joints against the requirements of the aerospace and military community, while focusing on the rework of SnPb and lead-free solder alloys and includes the mixing of SnPb and lead-free solder alloys. The majority of testing being conducted for this effort will mirror the testing completed for JCAA/JGPP LFS Project. Some changes were made in order to optimize the usefulness of the data.

OBJECTIVE
In response to concerns about risks from lead-free induced faults to high reliability products, the NASA-DoD Lead-Free Electronics Project Consortium outlined a multi-year project to provide manufacturers and users with data to clarify the risks of lead-free materials in their products. The project also provides useful data to component manufacturers supplying to high reliability markets. The project was launched in November 2006. The primary technical objective of the project is to undertake comprehensive testing to generate data on failure modes / criteria to better understand the reliability of packages (e.g., thin small outline package, ball grid array, plastic (dual inline package), chip scale package, quad flat pack (no leads) assembled and reworked with lead-free alloys and with mixed (lead/lead-free) alloys).

The intended goal of this project is to:

1. Determine the reliability of reworked solder joints in high-reliably military and aerospace electronics assemblies.
2. Assess the process parameters for reworking high-reliability lead-free military and aerospace electronics assemblies.

Develop baseline recommendations for process guidelines and a risk assessment for assembling high-reliability lead-free military and aerospace electronics assemblies.

PROCEDURES
Test Vehicle
The test vehicle is a printed wiring assembly (PWA), designed to evaluate solder joint reliability. Test vehicle raw boards comply with IPC-6012 (Qualification and Performance Specification for Rigid Printed Boards), Class 3, Type 3. Test vehicle size is 14.5 X 9 X 0.09 inches with six 0.5-ounce copper layers. The design incorporates components representative of the parts used for military and aerospace systems and is designed to reveal relative differences in solder alloy performance. A variety of plated through-hole (PTH) and surface mount technology (SMT) components are included. All components are "dummy" devices with pins internally daisy-chained and contain simulated die. The circuit board was designed with daisy-chained pads that are complementary to the components. Therefore, the solder joints on each component will be part of a continuous electrical pathway that can be monitored during testing by an event detector (Anatech or equivalent). Failure of a solder joint on a component will break the continuous pathway and be recorded as an event. Each

component has its own distinct pathway (channel). Figure 1 illustrates the test vehicle design.

Figure 1 Test Vehicle Design

All test vehicles were assembled using immersion silver (Ag) and a limited number of electroless nickel / immersion gold (ENIG) finished glass fiber (GF) laminate (IPC-4101/26) printed circuit boards with a glass transition temperature, T_g, of 170°C minimum and categorized as either "Manufactured" or "Rework". "Manufactured" test vehicles represent printed wiring assemblies newly manufactured for use in new product. Test vehicles being subjected to thermal cycle and combined environments testing will include forward and backward compatibility. Test vehicles assembled for vibration and mechanical shock will not include forward and backward compatibility. "Rework" test vehicles represent printed wiring assemblies manufactured and reworked prior to being tested. Solder mixing will be comprised of forward and backward compatibility:

1. Forward compatibility is a SnPb component attached to a printed wiring assembly using lead-free solder with a lead-free profile.
2. Backward compatibility is a lead-free component attached to a printed wiring assembly using SnPb solder with a SnPb solder profile.

In addition to the NASA-DoD Lead-Free Electronics Project test vehicles, Crane Division, Naval Surface Warfare Center, a NASA-DoD Consortium member, added 30 test vehicles to the NASA-DoD project in support of their Naval Supply Command (NAVSUP) sponsored "Logistics Impact of Lead-Free Circuits/Components" project. The primary purpose of the 30 test vehicle add-on was to perform multiple pass SnPb rework 1 and 2 times on random Pb-free DIP, TQFP-144, TSOP-50, LCC and QFN components from SAC305 and SN100C soldered assemblies.

The reworked test vehicles will be integrated into the NASA-DoD Lead-Free Electronics Project -55°C to +125°C thermal cycling testing (Rockwell Collins; Cedar Rapids, Iowa). Drop testing (Celestica; Toronto, Ontario, Canada) was run as an identical parallel test to minimize variation between the NASA-DoD and Crane test data. Celestica (Toronto, Ontario, Canada) also performed the vibration testing for the Crane test vehicles.

The goal of the Crane test vehicle effort is to generate initial data supporting the qualification of existing SnPb rework procedures for all military hardware built with lead-free processes through analysis of thermal cycling, vibration, and drop test data, with subsequent microsection analysis. Questions to be answered by the Crane testing effort include:

1. What effect does X1 and X2 rework have on assembly reliability as tested by thermal cycle, vibration, and drop testing?
2. Are lead-free assemblies reworked with SnPb as reliable as as-built lead-free hardware?
3. How do residual Pb-free solder contamination levels in SnPb joints after X1 and X2 rework correlate to reliability?
4. What effect does X1 and X2 SnPb rework have on surface mount land thickness (copper erosion) by cross section?
5. Observed visual evidence of X1 and X2 rework damage to 170Tg laminate?

All test results from the NASA-DoD Lead-Free Electronics Project and Crane Division, Naval Surface Warfare Center effort will be made publicly available on the NASA TEERM website [1].

Test Components

A variety of component types and component finishes were included on the test vehicle. The CLCC and TSOP component types were selected due to industry acknowledged solder joint integrity issues in Class III High Performance electronic products. The DIP components were selected to represent plated through-hole technology. The PLCC, TQFPs BGAs, CSPs and QFNs (MLF) were selected to represent surface mount technology. Table 1 lists the various component types with their associated surface finishes.

20LCC-1.27mm-8.90mm-DC-L-Au = **Tinning-SAC305**
20LCC-1.27mm-8.90mm-DC-L-Au = **Tinning-SnPb**
A-MLF20-5mm-.65mm-DC(30467)
A-MLF20-5mm-.65mm-DC-Sn(30801)
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643)
A-TQFP144-20mm-.5mm-2.0-DC-NiPdAu
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643) = **Tinning-SAC305**
A-TQFP144-20mm-.5mm-2.0-DC-Sn(30643) = **Tinning-SnPb**
PBGA225-1.5mm-27mm-DC(10565)
PBGA225-1.5mm-27mm-DC-LF(16074)
A-PDIP20T-7.6mm-DC-Sn (30737)
PDIP20T-DC (12006)
PDIP-20 - NiPdAu
A-CABGA100-.8mm-10mm-DC(30102)
A-CABGA100-.8mm-10mm-DC-LF(30695)
A-CABGA100-.8mm-10mm-DC-105
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-TR
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-SnBi-TR
A-TII-TSOP50-10.16x20.95mm-.8mm-DC-Sn-TR

Table 1 Component Types and Finishes

Destructive Physical Analysis (DPA) is being performed on samples from each of the component types being placed onto the test vehicles. The DPA process is being used to ensure that the components being used for testing meet the consortia required standards and to evaluate the quality of construction.

Test Vehicle Assembly

The test vehicles (193 in total) were assembled at the BAE Systems Irving, Texas facility. A detailed description of the specific tin/lead and lead-free soldering processes was detailed in the NASA-DoD Lead-Free Electronics Project Plan [2].

The lead-free solder alloys selected for this project were:

1. SAC305 – Sn3.0Ag0.5Cu – reflow soldering {Tin (Sn); Silver (Ag); Copper (Cu)}
2. SN100C – Sn-0.7Cu-0.05Ni + Ge – reflow and wave soldering {Tin (Sn); Copper (Cu); Nickel (Ni); Germanium (Ge)}

Sn37Pb was used as the baseline for reflow and wave soldering.

Table 2 lists the solder alloys used for each type of solder process during the assembly of the NASA-DoD Lead-Free Electronics Project test vehicles.

Selection criteria of prime importance included commercial availability, industry trends, and past reliability testing performance.

Solder Alloy	Solder Process		
	Reflow	Wave	Manual
SAC305	X	N/A	X
SN100C	X	X	X
SnPb baseline	X	X	X

Table 2 Solder Alloys and Processes

{N/A = Due to limitations on board numbers and components, these solder alloys were not used during the noted assembly processes}

Test vehicles were assembled using these solders and a variety of component types. The following harsh environment testing was then conducted:

1. Vibration (Boeing; Seattle, Washington and Celestica; Toronto, Ontario, Canada)
2. Thermal Cycle -20 to +80°C (Boeing; Seattle, Washington) and -55 to +125°C (Rockwell Collins; Cedar Rapids, Iowa)
3. Combined Environments Testing (Raytheon; McKinney, Texas)
4. Mechanical Shock (Boeing; Seattle, Washington)
5. Drop (Celestica; Toronto, Ontario, Canada)
6. Interconnect Stress Test (PWB Interconnect Solutions Inc.; Nepean, Ontario, Canada)
7. Copper Dissolution (Celestica; Toronto, Ontario, Canada and Rockwell Collins; Cedar Rapids, Iowa)

Table 3 lists the various categories of test vehicles that were assembled for this effort.

Test Vehicle Type	Reflow Solder	Wave Solder	Number of Boards
Lead-Free Rework All Test Vehicles	SAC305	SN100C	33
SnPb Rework* All Test Vehicles	SnPb*	SnPb*	40
SnPb Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SnPb	SnPb	17
SnPb Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SnPb	SnPb	17
Lead-Free Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SAC305	SN100C	20
Lead-Free Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SAC305	SN100C	43
Lead-Free Manufactured Test Vehicles Thermal Cycle and Combined Environments Tests	SN100C	SN100C	11
Lead-Free Manufactured Test Vehicles Vibration, Mechanical Shock and Drop Tests	SN100C	SN100C	6
Lead-Free Manufactured Test Vehicles Crane Rework Effort	SN100C	SN100C	6

Table 3 Test Vehicle Assembly Details

{* NOTE: Lead-Free profiles will be used for reflow and wave soldering}

The solder joint quality and placement accuracy of all test vehicles were x-ray and visually inspected in accordance with the IPC-JSTD-001 and IPC-A-610 specifications.

Test Vehicle Rework

There was a large volume of rework for this project. In order to get the rework procedures completed in a timely manner, multiple facilities performed the rework activities (BAE Systems; Irving, Texas, Lockheed Martin; Ocala, Florida, and Rockwell Collins; Cedar Rapids, Iowa).

Components reworked were grouped by rework solder alloy / material (SnPb, Flux only, SAC305 and SN100C). The location performing the rework chose what order to rework the solder alloy / material groups, but had to use the numbered order below for specific component locations within the solder alloy / material group. When reworking a component, the component was to be removed and replaced before moving to the next component. All details regarding the rework procedure, including temperature profiles, are contained in the NASA-DoD Lead-Free Electronics Project Plan.

Thermal Aging

The project consortia members desired to have the test vehicles begin the various testing procedures with a common starting state point in an effort to eliminate potential assembly differences which could possibly inadvertently/unintentionally influence the testing results. The project consortia members reviewed intermetallic calculations generated by Rockwell Collins and compared the calculations to data sets from the Center for Advanced Vehicle Electronics (CAVE) at Auburn University, the National Physics Laboratory (NPL), the National Institute of Standards and Technology (NIST), and the Center for

Advanced Life Cycle Engineering (CALCE) at University of Maryland.

The thermal aging procedure was selected to establish a common, standard starting point such that all test vehicles were relatively equal in terms of solder joint microstructure, printed wiring board stress state, surface finish oxidation condition, and intermetallic phase formation/thickness. The thermal aging procedure is not necessarily, nor intended to be, representative of the various burn-in, bake-out, or other environmental stress screening (ESS) procedures that are used to evaluate electronics hardware quality/functionality. Additionally, it should be noted that the thermal aging procedure being used by the NASA-DoD LFE Project consortia is not meant to be representative of operational field life.

Assembly Irregularities

With all of the complexities built into the NASA-DoD Lead-Free Electronics Project design of experiment, test vehicle irregularities were bound to occur.

When reviewing the CSP data, please note that the CSP components on all test vehicles only have continuity in the outside solder balls. The wrong component configuration was used during test vehicle drafting. Traces interconnecting internal rows of balls to the outside row of balls do not exist on the test vehicles, Figure 2

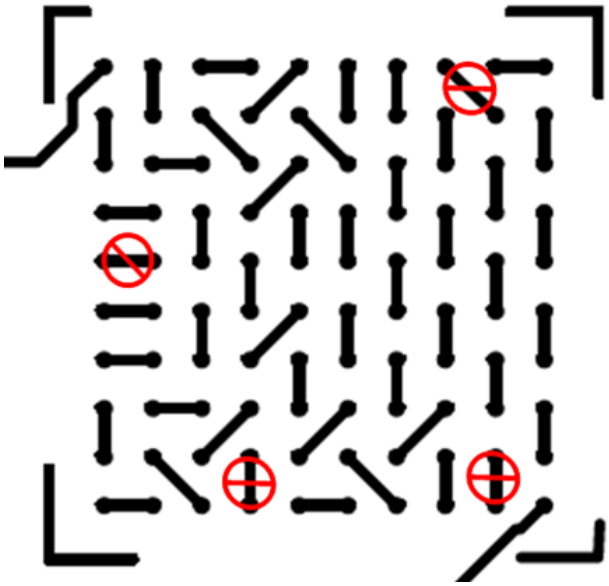

Figure 2 Test Vehicle Drawing, Chip Scale Package (CSP)

In order for a CSP component failure to be recorded, breaks in both sides of the continuity box must occur, Figure 3.

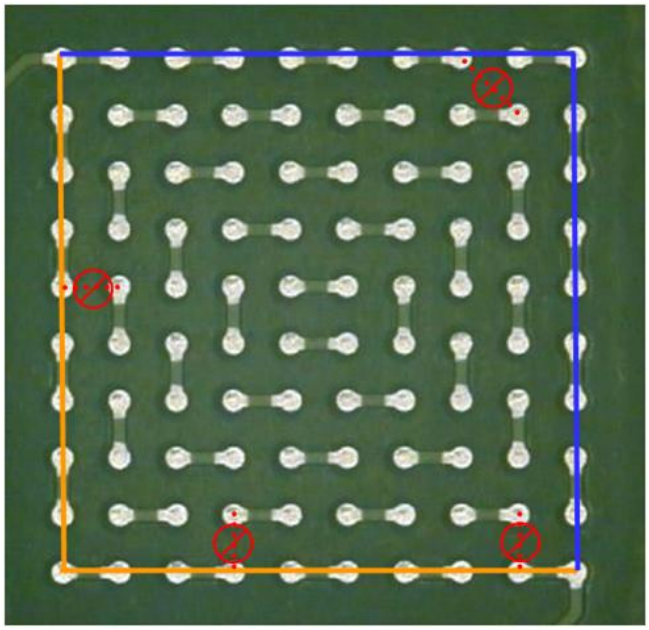

Figure 3 Chip Scale Package (CSP) Continuity Loop

The assembled boards were then subjected to harsh environments testing (e.g., thermal cycle, vibration, drop, mechanical shock) to better define solder joint reliability. Results from the project have been made available during the duration of the project allowing advanced information to assist organizations in their implementation or mitigation strategies.

TESTING PARAMETERS AND METHODOLOGY

In developing the test plan, there was a review of the performance requirements called out in applicable military and industry standards. The next step was to select test methods recognized and agreed upon by the technical team members. A key factor was selecting test parameters that would subject enough environmental stress to cause solder joints to fail, thus permitting differentiation between lead vs. lead-free performance. Military document MIL-STD-810F [3] and industry documents IPC-SM-785 [4] and IPC-TM-650 [5] were primary references used for writing the test plan. One test—the Combined Environments test—followed a procedure developed and used by Raytheon.

Vibration (Boeing; Seattle, Washington and Celestica; Toronto, Ontario, Canada)

The vibration test was conducted at two separate locations. The NASA-DoD Lead-Free Electronics Project test vehicles were tested at Boeing while the Crane Division test vehicles were tested at Celestica.

The vibration test determines solder joint failures during exposure to vibration conditions. The stakeholders agreed that MIL-STD-810F, Method 514.5 (Vibration), would be the starting point for developing a vibration test that would determine the reliability of the various solder alloys under severe vibration. Specific details on the vibration test can be found in the Joint Test Protocol [6].

The stakeholders agreed that a stress step test representing increasingly severe vibration environments was appropriate for this test, see Figure 4. A step stress test is required since a test conducted at a constant 8.0 g_{rms} level (Step 1) would take thousands of hours to fail the same number of components as a step stress test. This is because some locations on a circuit assembly experience very low stresses and severe vibration is required in order to fail components at these locations. The shape of the PSD (Power Spectral Density) curve for each step stress level was designed so that all of the major resonances of the test vehicles would be excited by the random vibration input. The PSD curves presented in MIL-STD-810F were used as guides for the creation of this step stress test but were not directly duplicated.

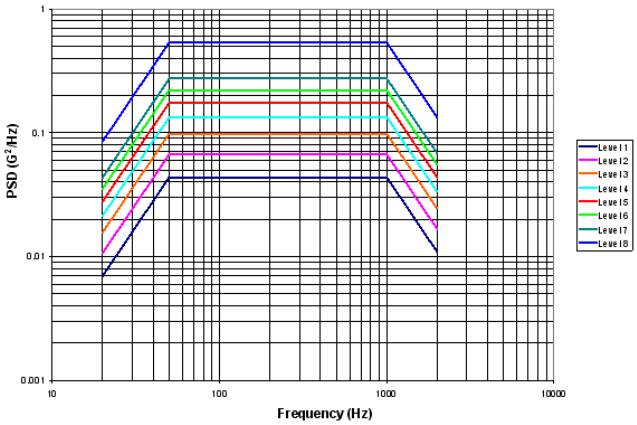

Figure 4 Vibration Spectrum

Thermal Cycle -20 to +80°C (Boeing; Seattle, Washington) and -55 to +125°C (Rockwell Collins; Cedar Rapids, Iowa)

The thermal cycle testing determines the capability of a solder to withstand extreme thermal cycling. This test will be performed in accordance with IPC-SM-785. Figure 5 illustrates the test vehicles loaded into the -55 to +125ºC test chamber.

Thermal cycling will be conducted at two different conditions, -20 to +80°C and -55 to +125°C, technical representatives from the U.S. Army Aviation and Missile Command (AMCOM) suggested two temperature ranges to allow for acceleration factors to be determined, which will permit extrapolation of the data to actual use conditions of their systems. The thermal cycle tests were run until a significant number (greater than 63 percent) of component failures were achieved in order to provide statistically meaningful data. Specific details on the thermal cycle test can be found in the Joint Test Protocol.

After examining the available data on dwell time effect, the lead-free solder project participants agreed that the high-temperature dwell time would be 30 minutes. Solder alloy creep during the high temperature dwell of the thermal cycle is largely responsible for damage within the solder joints. In order to maximize the effects of solder alloy creep, a 30-minute high temperature dwell will be used for this project.

Figure 5 Test Vehicles in the Thermal Cycle Chamber

Combined Environments Testing (Raytheon; McKinney, Texas)

The Combined Environments Test (CET) determines the reliability of solders under combined thermal cycle and vibration. The CET for the NASA-DoD Lead-Free Electronics Project is based on a modified Highly Accelerated Life Test (HALT), a process in which products are subjected to accelerated environments to find weak links in the design and/or manufacturing process. The project stakeholders felt that the CET would provide a quick method to identify comparative potential reliability differences in the test alloys vs. the SnPb baseline. The primary accelerated environments are temperature extremes (both limits and rate of change) and vibration (pseudo-random six degrees of freedom used in combination). Specific details on the combined environments test can be found in the Joint Test Protocol.

This test utilized a temperature range of –55 to 125°C with 20°C/minute ramps. The dwell times at each temperature extreme are the times required to stabilize the test sample plus a 15-minute soak. 10 g_{rms} pseudo-random vibration was applied for the duration of the thermal cycle. Testing continued until sufficient data was generated to obtain statistically significant Weibull plots indicating relative solder joint endurance (cycles to failure) rates. If significant failure rates were not evidenced after 50 cycles, the vibration levels were increased in increments of 5 g_{rms} and cycling continued for an additional 50 cycles. This process was repeated until all parts failed or 55 g_{rms} was reached. Figure 6 illustrates the test vehicles loaded into the HALT/HASS Chamber.

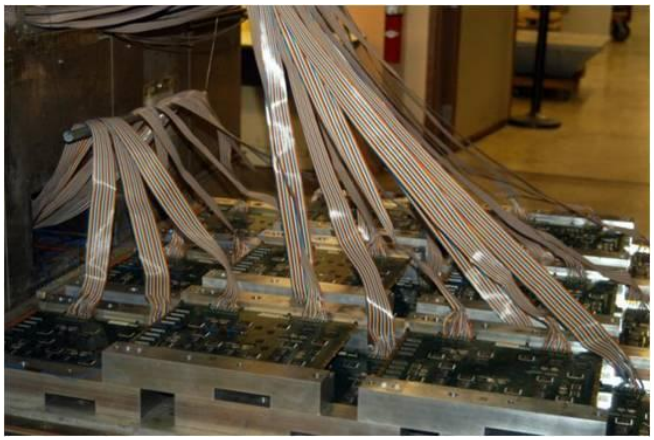

Figure 6 Test Vehicles in the HALT/HASS Chamber

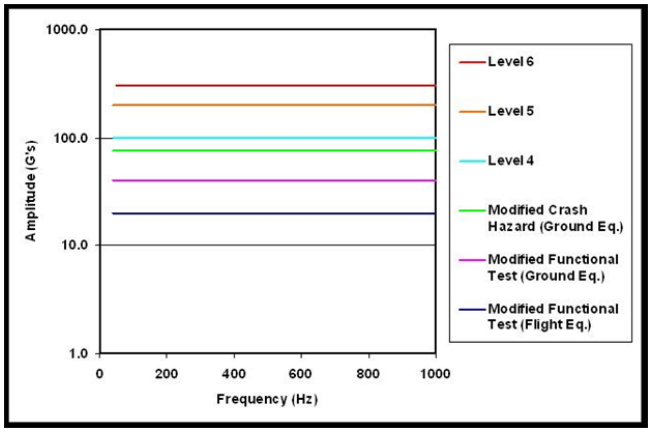

Figure 7 Mechanical Shock SRS Test Levels

Mechanical Shock (Boeing; Seattle, Washington)
The purpose of the mechanical shock test is to determine the resistance of the solder to the stresses associated with high-intensity shocks induced by rough handling, transportation, or field operation. The mechanical shock test procedure was changed from the procedure used for the JCAA/JGPP Lead-Free Solder Project. The consortia members felt that the procedure change was necessary since it is very difficult to meet both the SRS shape and the pulse duration for this test as outlined in MIL-STD-810F. Pulse duration is approximately equal to the inverse of lowest SRS frequency, 10 Hz. SRS requirement means pulse duration >100 msec while MIL-STD-810F outlines pulse durations $\leq$ 23 msec. Specific details on the mechanical shock test can be found in the Joint Test Protocol.

Testing followed MIL-STD-810F, Method 516.5 with the following modifications: (1)100 shocks were applied per test level (rather than 3) and all of the shocks were applied in the Z-axis, and (2) the shock transients applied at the levels specified in MIL-STD-810F, Method 516.5 for the Functional Test for Flight Equipment, the Functional Test for Ground Equipment, and the Crash Hazard Test for Ground Equipment followed modified parameters detailed in the Joint Test Protocol. An additional step stress test will then be conducted (see Figure 7) with the shocks being applied in the Z-axis only. For Level 6 (300 G's), 400 shocks will be applied instead of 100. Testing continued until a majority (approximately 63 percent) of components was failed.

Drop (Celestica; Toronto, Ontario, Canada)
This test determines the resistance of board level interconnects to board strain induced by dynamic bending as a result of drop testing. Boards tested using this method typically fail either as interfacial fractures in the solder joint (most common with ENIG) or as pad cratering in the component substrate and/or board laminate. These failure modes commonly occur during manufacturing, electrical testing (especially in-circuit test), card handling and field installation. The root cause of these types of failures is typically a combination of excessive applied strain due to process issues and/or weak interconnects due to process issues and/or the quality of incoming components and/or boards. Specific details on the drop test can be found in the Joint Test Protocol. Figure 8 illustrates the test vehicles loaded onto the drop test fixture.

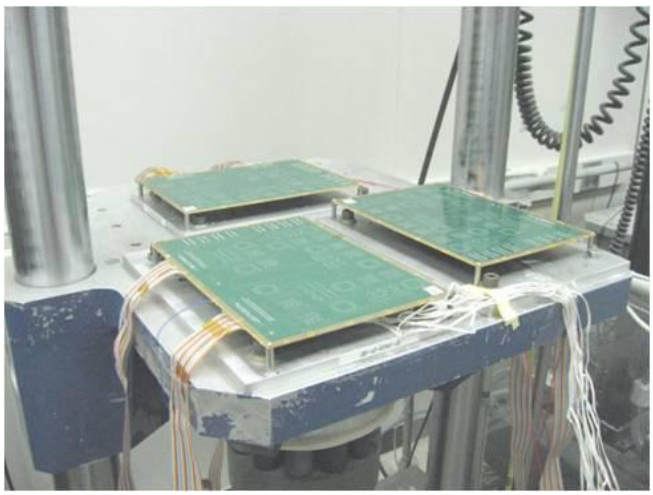

Figure 8 Test Vehicles on the Drop Test Fixture

Interconnect Stress Test (PWB Interconnect Solutions Inc.; Nepean, Ontario, Canada)
Interconnect Stress Test (IST) is an industry recognized test method (IPC) that accelerates thermal cycling testing by heating a specifically designed test coupon to 150°C in exactly 3 minutes followed by cooling to ambient in approximately two minutes. IST test coupons have two circuits, a sense circuit and a power circuit, to monitor

material delamination and crazing. The power circuit heats the coupon. The sense circuit is a passive circuit that monitors temperature and measures damage accumulation of the interconnect structure, typically a plated through-hole (PTH). There are usually 400 to 800 structures per circuit to achieve a higher, statistically relevant, sample size. Both the power and sense circuits change in resistance (milliohms) and temperature (°C) throughout the coupons during the thermal cycle. Thermal cycling continues until end of test or a 10% increase in resistance on either circuit. Each coupon is heated, monitored, and tested individually. This gives a number of advantages that include no hold time at temperature, tight test control in the ability to achieve any test temperature in three minutes +/- 5 seconds, the ability to stop testing within seconds of the circuit achieving a 10% increase in resistance allowing analysis of a developing failure rather than a catastrophic failure. Testing stops immediately when the circuit achieves 10% increase in resistance, allowing a failed circuit to have a low amount of power applied that creates a hot spot at the failure site visible by a thermal imaging camera. Specific details on IST can be found in the Joint Test Protocol.

Copper Dissolution (Celestica; Toronto, Ontario, Canada and Rockwell Collins; Cedar Rapids, Iowa)

The purpose of the copper dissolution testing is to characterize, document, and compare the impact of soldering process on the copper plated through-hole and surface pad structures for the NASA-DoD test vehicles with the SAC305 and SN100C solder alloy systems. The copper dissolution test results will provide a data set which can be used as a first order approximation of the copper plating thickness loss due to lead-free solder processing. Additionally, the copper dissolution test results can be compared to other published industry results for alternative solder alloy systems and different soldering processes.

Printed Circuit Board (PCB) and plated through-holes can be eroded or dissolved away in the presence of molten solder rendering the PCB non-functional. Significant dissolution can occur with the use of certain new Sn-rich alloys and is further exacerbated by higher process temperatures. Clearly this phenomenon represents a serious risk to circuit reliability. There is a clear need to determine the dissolution rate of copper pads with lead-free solders under various conditions. Specific details on copper dissolution can be found in the Joint Test Protocol.

TEST RESULTS

At the time this document was drafted, only a portion of the testing activities had been completed. For the testing activities that were complete, failure analysis activities were ongoing or in the planning stages. All test reports will be made available on the NASA TEERM website.

DISCUSSION

Based on the work that has been completed to date, assembly of high-performance electronics using lead-free solder alloys is possible without a total retrofit of the factory.

Some control of equipment is necessary to eliminate the cross contamination of lead-free and SnPb solder alloys to ensure optimal reliability for some component types. Significant resources will be required for component configuration management to assure that incompatible metallurgies are not mixed in the factory. The huge potential for mixed components from suppliers will drive validation and inspection costs throughout the factory.

FUTURE WORK

For the testing activities that have been completed, failure analysis activities are schedule to be conducted later this year.

The thermal cycle testing (-20 to +80^{o}C and -55 to +125^{o}C) was on going at the time this paper was drafted. -55 to +125^{o}C testing is expected to be completed over the summer with data and failure analysis to be completed later in the year. It is unknown when the -20 to +80^{o}C testing will be complete.

ACKNOWLEDGEMENTS

The author would like to thank Lety Campuzano-Contreras of BAE Systems; Dr. Tom Woodrow of Boeing; Dave Hillman of Rockwell Collins; Cynthia Garcia and Jeff Bradford of Raytheon; Dr. Polina Snugovsky, Jason Bragg, and Jeff Kennedy of Celestica; Linda Woody and Ed Morris of Lockheed Martin; Paul Reid and Bill Birch of PWB Interconnect Solutions Inc; Jim Blanche of Jacobs Engineering; Vance Anderson of Defense Microelectronics Activity; Andy Ganster and Gary Latta of Crane Division, Naval Surface Warfare Center and David Amidei and Chuck Griffin of NASA.

The author would also like to acknowledge the other members of the NASA-DoD Lead-Free Electronics Consortium not mentioned by name. This effort would not be possible without their contributions.

REFERENCES

[1] NASA Technology Evaluation for Environmental Risk Mitigation (TEERM) Principal Center website; http://teerm.nasa.gov

[2] NASA-DoD Lead-Free Electronics Project Consortium, "NASA-DoD Lead-Free Electronics Project Plan"; March 2010

[3] MIL-STD-810F: Environmental Engineering Considerations and Laboratory Tests January 2000

[4] IPC SM 785: Guidance for Accelerated Reliability Testing of Surface Mount Solder Attachments Nov. 1992

[5] IPC TM 650: Test Methods Manual January 2007

[6] NASA-DoD Lead-Free Electronics Project Consortium, "NASA-DoD Lead-Free Electronics Project, Joint Test Protocol"; September 2009